REMARKS

This paper is responsive to an Office Action mailed March 10, 2006. Prior to this response, claims 16-17 and 20-28 were pending. Claim 16-17 and 20-28 remain pending.

In Section 5 of the Office Action claims 16-17, 20-22, and 25-27 have been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal (US 6,451,641), in view of King (US 6,754,104) and Kirkpatrick (US 4,197,144). With respect to claim 16, the Office Action acknowledges that Halliyal does not describe the steps of inducing trapping centers in a dielectric material, in response to an ionized species exposure. The Office Action also states that it would have been obvious at the time of the invention to induce trapping centers into a dielectric material, as suggested by King and Kirkpatrick, to increase the number of storage sites within the dielectric layer. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in

the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

Halliyal generally describes a MOS transistor made with a high-k dielectric (Abstract). The novelty of Halliyal's invention appears to be a method of forming a polySi gate electrode that does not "reduce" the underlying high-k dielectric gate insulator (col. 5, ln. 27-46). Halliyal does not describe either a NROM or MONOS memory device, or any kind of transistor that operates on a charge trapping or floating gate principle. More particularly, Halliyal does not describe the steps of exposing a high-k dielectric material to an ionized species, inducing charge trapping centers in the high-k dielectric material as a result of the exposure, or a device where charge can be trapped in a gate stack.

Generally, King discloses processes for forming an integrated gate FET (IGFET) and a negative differential resistance (NDR) FET using common processing operations (Abstract). King states that a first electrically insulating layer 1020 (e.g., a high permittivity dielectric) is formed over a substrate. King states that it is desirable to induce trapping centers in the insulating layer 1020, by ion implantation or diffusion (col. 14, ln. 4-20). Ions such as boron, indium, arsenic, phosphorus, fluorine, chlorine, or germanium are selectively implanted in either the substrate, or into the areas where the FETS are to be formed (col. 14, ln. 31-51). As noted in the affidavit accompanying this response, it is the opinion of Dr. David R. Evans that King uses change trapping for the purpose of inducing a negative differential resistance, and that King's charge trapping centers cannot be used for non-volatile purposes. That is, King's NDR FET does not store a memory state (charge).

Generally, Kirkpatrick discloses an ion implantation process for forming charge trapping sites into an insulator material. Kirkpatrick notes that a memory can be enabled by reading charge storage variations in the oxide electrode insulator of a planar *diode* structure (col. 1, ln. 11-31). Kirkpatrick explicitly describes such a diode device having a pn junction 11/12, an oxide layer 14, and a conductive electrode layer 15. At col. 4, ln. 5, Kirkpatrick discloses implanting a silicon dioxide insulator with Si ions. Unlike the claimed invention, which recites forming charge trapping centers in a high-k dielectric, Kirkpatrick discloses a silicon dioxide insulator. Unlike, the claimed invention, which recites a transistor memory device, Kirkpatrick discloses a diode memory.

With respect to the first *prima facie* requirement, there must be some suggestion in the King and Kirkpatrick references to modify Halliyal in a manner that makes the claimed invention obvious. The Office Action states that it would have been obvious to combine the references, to increase the number of storage sites within the dielectric layer. However, the Applicant respectfully submits that such a rationale can only be constructed in hindsight, in light of the claimed invention. That is, it appears as if the references were chosen as a result of a search using limitations from the claimed invention as keywords. No evidence has been provided of particular features from either the King or Kirkpatrick disclosures that would suggest modifications to Halliyal. Broadly, Kirkpatrick is the only reference that specifically mentions a memory application, and there is no evidence to suggest that a process that protects a high-k dielectric from reduction (Halliyal), a NDR FET, and a memory diode suggest a method of increasing the number of storage sites in a dielectric layer, as suggested in the Office Action.

Considered from the perspective of the second *prima facie* requirement, even if an expert were given the three references as a foundation, there is no reasonable expectation that this expert could derive the claimed invention, since none of the references suggest the claimed gate stack structure. That is, none of the reference discloses a memory transistor with charge trapping region formed from a single layer of high-k dielectric (without an underlying or overlying oxide layer).

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. Applicant's claim 16 recites the steps of forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. As noted above, Halliyal does not address the subject of charge trapping or of a memory FET. King does not address the use of charge traps for memory applications. Kirkpatrick does not describe a transistor memory or a high-k dielectric material. Therefore, the combination of references does not explicitly describe all the steps of claim 16. Neither does the combination of references suggest any modifications that make these limitations obvious. Claims 17, 20-22, and 25-27, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 15 of the Office Action claim 23 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Chooi (US 6,486,080) and Agarwal (US 2001/0015453). The Office Action acknowledges that Halliyal/King/Kirkpatrick do not describe a densification annealing, but that Chooi and Agarwal do. The Office Action states that it would have been obvious to follow the deposition of the Halliyal/King/Kirkpatrick

trapping layer with an annealing to cure oxygen vacancies. This rejection is traversed as follows.

At col. 6, ln 5-7, Chooi describes the densification of a metal oxide. At paragraph [0005] Agarwal describes densification to cure oxygen vacancies in a high-k dielectric. It is not clear how these references have any application to the claimed invention, which performs a densification annealing to prevent delamination of the gate (specification, page 12, ln. 24-25). Further, neither of these references describes ion implantation processes, the use of a high-k dielectric as a charge trapping material, or the use of a high-k dielectric memory device. These references do not suggest any modifications to the King/Kirkpatrick ion implantations. Likewise, these references do not suggest modifications to Halliyal's high-k dielectric reduction protection process.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 23, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 17 of the Office Action claim 24 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Liang (US 5,372,957). The Office Action acknowledges that Halliyal/King/Kirkpatrick do not describe a drain/source angle implant, as described by Liang. The Office Action

states that it would have been obvious to form Halliyal's source/drain regions using Liang's process, to protect the transistor from hot carrier degradation. This rejection is traversed as follows.

Even if Liang does describe an angle implant to form source/drain regions, it is not apparent that Liang suggests any modifications to the ion implantation processes of either King or Kirkpatrick, or to Halliyal's high-k dielectric reduction protection process.

With respect to the third *prima facie* requirement, the combination of references does not disclose all the elements of the claimed invention. Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 24, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

In Section 19 of the Office Action claim 28 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Moslehi (US 5,372,957). The Office Action acknowledges that Halliyal/King/Kirkpatrick do not describe generating plasma using an ICP source, as described by Moshehi.

However, even if the above-mentioned references can be combined, they do not disclose all the elements of the claimed invention. With respect to the third *prima facie* requirement, Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the

combination of references suggest any modifications that make these limitations obvious. Claim 28, dependent from claim 16, enjoys the same distinctions from the cited prior art, and the Applicant requests that the rejection be removed.

It is believed that the application is in condition for allowance and reconsideration is earnestly solicited.

Respectfully submitted,

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